IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants:	Behrens et al.
Serial No.:	10/032,513
For:	DATA FLOW SYNCHRONIZATION
Filed:	26 OCT 2001
Examiner:	Juan A. Torres
Art Unit:	2611
Confirmation No.:	6890
Customer No.:	27,623

Attorney Docket No.: 20 01 0631

APPEAL BRIEF FILED UNDER 35 U.S.C. §134

Mail Stop Appeal Brief - Patents
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants are filing this Appeal Brief under 35 U.S.C. §134 and in accordance with the provisions of 37 C.F.R. §41.37(a), and believe that the Appeal Brief complies with the requirements set forth in 37 C.F.R. §41.37(c). The claims on appeal are set forth in an Appendix, below.

The Commissioner is hereby authorized to charge Deposit Account No. 01-0467 in the name of Ohlandt, Greeley, Ruggiero & Perle for any required fee not submitted herewith, or submitted incorrectly, so as to maintain the pendency of the above-identified patent application.

04/16/2007 SSESHE1 00000061 10032513
01 FC:1402 500.00 OP

(1) Real Party in Interest

The real party in interest is Verigy (Singapore) Pte. Ltd.

(2) Related Appeals and Interferences

The undersigned attorney is not aware of any related appeals or interferences.

(3) Status of the Claims

Claims 1 - 11 are pending in this application, and are the subject of this Appeal.

In an Office Action mailed 28 SEP 2006 (hereinafter "the Office Action"), the Examiner made final his rejection of claims 1 - 11 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,324,664 to Farwell et al. (hereinafter "the Farwell et al. patent") in view of U.S. Patent No. 6,055,285 to Alston (hereinafter "the Alston patent"). No claims are canceled, withdrawn or objected to.

(4) Status of Amendments

No amendments to any claims were proposed subsequent to final rejection.

(5) Summary of Claimed Subject Matter

The application contains one figure. A copy of the figure is provided below, at the end of the Summary.

The present invention relates to synchronizing a data flow between devices. For testing digital circuits, a device under test (DUT) typically receives a stimulus signal, and a response signal of the DUT on the stimulus signal is determined and e.g. compared with an expected response signal. Thus, errors can be determined e.g. when the determined response signals deviates from the expected response signal.

The figure (provided below) shows an embodiment of a testing unit 10. A signal generator 20 provides a stimulus signal to a device under test DUT 30. A signal response of the DUT 30 on the stimulus signal is provided via a synchronizing unit 40 to a receiving unit 50. An analyzing unit 60 compares the response signal as received by the receiving unit 50 with an expected response signal for determining whether the DUT 30 behaves in the expected way or whether errors occur.

The synchronizing unit 40 receives a clock signal DUT-CLK from the DUT 30 and a clock signal CLK of the testing unit 10. The synchronizing unit 40 provides synchronization between the provision of the response signal from the DUT 30 and the receiving of the corresponding response signal by the receiving unit 50. Thus, it can be ensured that a certain event within the response signal from the DUT 30 can be unambiguously assigned to a corresponding event in the expected response signal, so that temporal mismatches between the actual and the expected response signal can be avoided, and that only corresponding events within the actual and expected response signal will be compared by that analyzing unit 60.

The synchronizing unit 40 comprises a delay unit 70 having a structure with a plurality of individual registers 70A-70H. A write unit 80 receives the response signal from the DUT 30 and successively writes successive data words of the response signal into successive registers of the delay unit 70. Accordingly, a read unit 90 successively reads out successive data words of the response signal as stored in the delay unit 70 and provides those data words to the receiving unit 50.

The delay unit 70 in conjunction with the write unit 80 and the read unit 90 preferably provides a FIFO structure, wherein the individual registers of the delay unit 70 are repeatedly written and read out e.g. in a circular manner as indicated in the figure. For that purpose, a write pointer 100 of the write unit 80 is repeatedly moved between the registers 70A-70H, so that the registers of the delay unit 70 will be rewritten with each writing cycle. Accordingly, a read pointer 110 is moved repeatedly between the registers 70A-70H.

The write accesses as provided by the write pointer 100 have to stay within limits in relation to the read accesses as provided by the read pointer 110, so that it is, on one hand, avoided that the write unit 80 will overwrite data in the delay unit 70 before it has been read out by the read unit 90, and, on the other hand, that it is avoided that the read unit 90 reads faster than the write unit 80 can write, so that the read unit 90 will virtually "overtake" the write unit 80. For that purpose, the clock rates DUT-CLK and CLK should be synchronized.

An initial delay time between corresponding read and write accesses will be set to half of the number of registers in the delay unit 70. For testing unit 10, the initial delay time will be set to four registers. That means that while the write unit 80 e.g. writes to register 70F, the read unit 90 initially reads out register 70B.

The present application contains two independent claims, namely claims 1 and 8. Below, Appellants are providing a concise explanation of the subject matter defined in each of the independent claims. The explanation refers to the specification (as filed) by page and line number, and to the figure by reference number.

Claim 1 provides for a testing unit 10 for testing a device under test (DUT) 30. The testing unit 10 includes:

a signal generator 20 that applies a stimulus signal to the DUT 30 (page 4, lines 12 - 13);

a receiving unit 50 that receives a response signal from the DUT 30 on the applied stimulus signal (page 4, lines 13 - 14); and

a synchronizing unit 40 that synchronizes a data flow of the response signal between the DUT 30 and the receiving unit 50 (page 5, lines 1 - 3);

wherein the synchronizing unit 40 receives a first clock signal (DUT-CLK) from the DUT and a second clock signal (CLK) from the testing unit 10 (page 4, lines 23 - 24); and

wherein the synchronizing unit 40 includes:

a buffer (delay unit 70) for buffering data (Abstract, and page 5, lines 9 - 12);

a write unit 80 for writing data from the DUT 30 into the buffer (delay unit 70) (page 5, lines 12 - 14), wherein the first clock signal (DUT-CLK) controls a write access onto the buffer (delay unit 70) (page 6, lines 16 - 19); and

a read unit 90 for reading out data from the buffer (delay unit 70) to be provided to the receiving unit 50 (page 5, lines 14 - 16), wherein the second clock signal (CLK) controls a read access onto the buffer (delay unit 70) (page 6, lines 19 - 20).

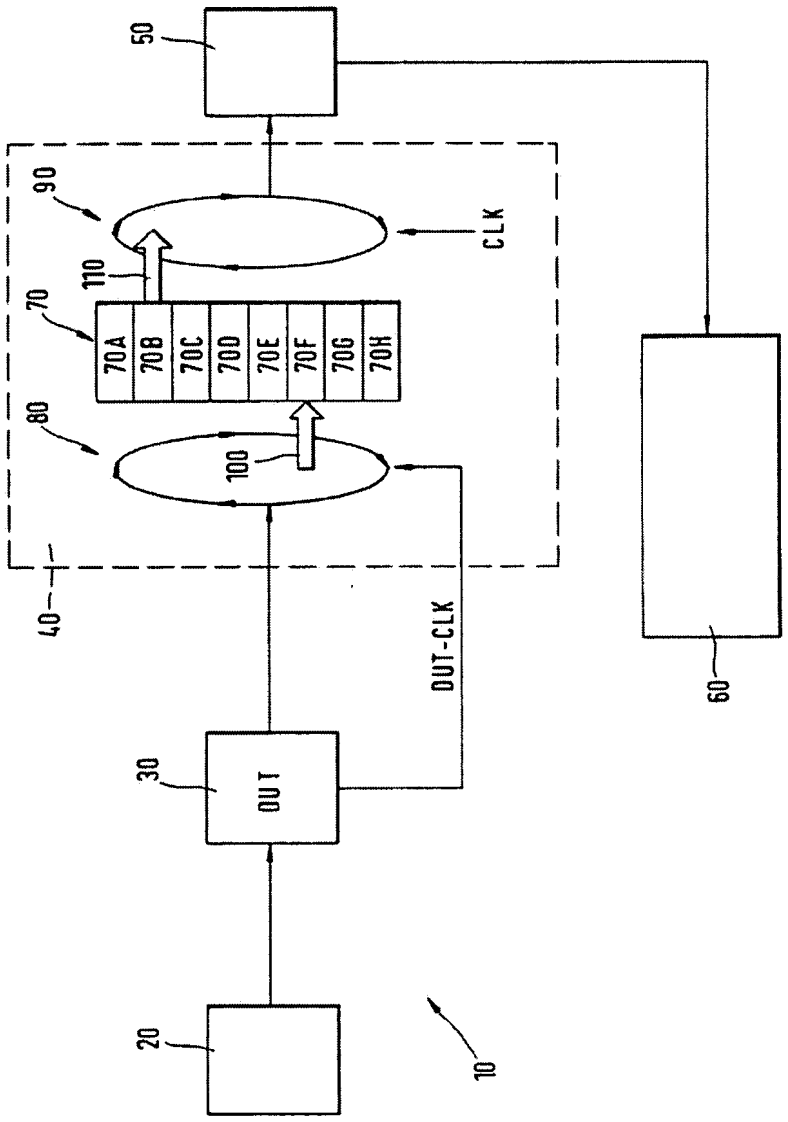
Claim 8 provides for a method for testing a device under test (DUT) 30, the method comprising:

applying a stimulus signal to the DUT 30, wherein the DUT 30 outputs data in response to the stimulus signal (page 4, lines 12 - 14);

writing the data into a buffer (delay unit 70) (Abstract, and page 5, lines 9 - 12), wherein the writing employs a first clock signal (DUT-CLK) that controls a write access of the buffer (delay unit 70) (page 6, lines 16 - 19), and wherein the first clock signal (DUT-CLK) is provided by the DUT 30 (page 4, lines 23 - 24);

reading the data from the buffer (delay unit 70) (page 5, lines 14 - 16), wherein the reading employs a second clock signal (CLK) that controls a read access of the buffer (delay unit 70) (page 6, lines 19 - 20), and wherein the second clock (CLK) is provided by a receiving unit 50 (page 4, lines 23 - 24, and lines 26 - 27); and

communicating the data from the buffer (delay unit 70) to the receiving unit 50 (page 5, lines 14 - 16).


50
90
CLK
110
70
70A
70B
70C
70D
70E
70F
70G
70H
80
100
40
DUT-CLK
60
30
DUT
20
10

(6) Grounds of Rejection to be Reviewed on Appeal

The issue presented for review is the propriety of the Examiner's final rejection of claims 1 - 11 under 35 U.S.C. §103(a) as being unpatentable over the cited combination of the Farwell et al. and Alston patents.

(7) Argument

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Furthermore, if an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

(a) Claims 1 - 11 stand or fall together.

As mentioned above, claim 1 provides for a testing unit for testing a device under test (DUT). The testing unit includes, *inter alia*, a synchronizing unit that receives a first clock signal from the DUT and a second clock signal from the testing unit. The synchronizing unit includes (a) a buffer for buffering data, (b) a write unit for writing data from the DUT into the buffer, wherein the first clock signal controls a write access onto the buffer, and (c) a read unit for reading out data from the buffer to be provided to a receiving unit, wherein the second clock signal controls a read access onto the buffer.

The Farwell et al. patent, with reference to FIG. 1, discloses an integrated circuit 10 coupled to external test equipment 33 via a test bus 31. Integrated circuit 10 includes combinatorial logic 15, a scan path 20, an output memory 25, a modulo counter 27, a read/write controller 19, and a test bus controller 29. A system clock (SYSCLK) clocks modulo counter 27 and scan path 20 (see FIG. 1), and test bus controller 29 provides a TEST CLOCK to read/write controller 19 (col. 4, lines 6 - 8). Read/write controller 19 (i) evaluates an index provided by modulo counter 27 to enable output memory 25 to sample the output of scan path 20, i.e., to write data into output memory 25, and (ii) in cooperation with test bus controller 29[1] reads output memory 25 (col. 3, line 65 - col. 4, line 8; and col. 4, lines 25 – 45). The Farwell et al. patent, at col. 5, lines 33 - 38, states:

> A scan test circuit has been described that employs a continuous system clock (SYSCLK) and accommodates a test clock (TEST CLOCK) that can be discontinuous or asynchronous relative to the system clock, and advantageously provides for scan testing of an integrated circuit that employs dynamic logic. (Emphasis added)

The Alston patent is directed toward a synchronization circuit for transferring data between two asynchronous circuits (Abstract).

The Office Action, near the bottom of page 8, recognizes that the Farwell et al. patent does not specifically disclose that a first clock signal controls a write access into a buffer, and a second clock signal controls a read access onto the buffer. Therefore, the Office Action, on page 9, introduces the Alston patent, and states that it would have been obvious to supplement the apparatus disclosed by the Farwell et al. patent with the synchronization circuit disclosed by the Alston patent. The Office Action further indicates that the suggestion/motivation for combining the Farwell et al. and Alston patents would have been to synchronize the transfer of data.

However, whereas the Farwell et al. patent expressly states that the system accommodates asynchronous clocks, there is no apparent need to modify the Farwell et al. patent to include the synchronization circuit of the Alston patent. Moreover, if the Farwell et al. patent were modified to include the synchronization circuit of the Alston patent, such a modification would obviate the manner in which modulo counter 27 and test bus controller 29 coordinate the writing of data to, and reading of data from, output memory 25, thus changing the principle of operation of the Farwell et al. patent. Hence, the cited

[1] The Farwell et al. patent, at col. 4, line 44, refers to "test bus controller 27", but from FIG.1, it is clear that the Farwell et al. patent intended to refer to "test bus controller 29."

combination of the Farwell et al. and Alston patent is **improper for purposes of a section 103(a) rejection** of claim 1. Accordingly, Appellants submit that claim 1 is patentable over the cited combination of the Farwell et al. and Alston patents.

Claims 2 - 7 depend from claim 1. By virtue of this dependence, claims 2 - 7 are also patentable over the cited combination of the Farwell et al. and Alston patents.

Claim 8 includes a recital similar to that of claim 1, as presented above. Accordingly, claim 8, for reasoning similar to that provided in support of claim 1, is patentable over the cited combination of the Farwell et al. and Alston patents.

Claims 9 - 11 depend from claim 8. By virtue of this dependence, claims 9 - 11 are also patentable over the cited combination of the Farwell et al. and Alston patents.

In view of the foregoing arguments, Appellants respectfully requests that the Board of Appeals reverse the final rejection of claims 1 - 11 under 35 U.S.C. §103(a) as being unpatentable over the cited combination of the Farwell et al. and Alston patents, thereby enabling all of the pending claims to be allowed.

Respectfully submitted,

4/11/07
Date

Paul D. Greeley
Reg. No. 31,019
Attorney for the Appellants
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
One Landmark Square, 10th Floor
Stamford, CT 06901-2682
Tel: 203-327-4500
Fax: 203-327-6401

(8) Claims Appendix

The claims on appeal are set forth below.

1. (previously presented) A testing unit for testing a device under test (DUT), comprising:
a signal generator that applies a stimulus signal to the DUT,
a receiving unit that receives a response signal from the DUT on the applied stimulus signal; and
a synchronizing unit that synchronizes a data flow of the response signal between the DUT and the receiving unit;
wherein the synchronizing unit receives a first clock signal from the DUT and a second clock signal from the testing unit; and
wherein the synchronizing unit includes:
a buffer for buffering data;
a write unit for writing data from the DUT into the buffer, wherein the first clock signal controls a write access onto the buffer; and
a read unit for reading out data from the buffer to be provided to the receiving unit, wherein the second clock signal controls a read access onto the buffer.

2. (previously presented) The testing unit of claim 1, wherein the buffer comprises a register structure with a plurality of registers.

3. (previously presented) The testing unit of claim 2, further comprising:
a write pointer that moves between the pluralities of registers for defining one of the plurality of registers to receive and buffer data from the DUT; and
a read pointer that moves between the plurality of registers for defining one of the pluralities of registers to be read out.

4. (previously presented) The testing unit of claim 3, wherein the write pointer is clocked by the first clock signal for successively writing successive data words from the DUT to different registers, and the read pointer is clocked by the second clock signal for successively reading out successive data words buffered in the plurality of registers.

5. (previously presented) The testing unit of claim 1, wherein the write unit comprises a latch controlled by the first clock signal, so that successive data words can be latched with the first clock signal and thus successively written into the buffer.

6. (previously presented) The testing unit of claim 1, wherein the buffer provides an initial delay time between a first valid write access and a first valid read access.

7. (previously presented) The testing unit of claim 6, wherein the initial delay time is dependent on a maximum expected variation between such write and read accesses.

8. (previously presented) A method for testing a device under test (DUT), the method comprising:

applying a stimulus signal to the DUT, wherein the DUT outputs data in response to the stimulus signal;

writing the data into a buffer, wherein the writing employs a first clock signal that controls a write access of the buffer, and wherein the first clock signal is provided by the DUT;

reading the data from the buffer, wherein the reading employs a second clock signal that controls a read access of the buffer, and wherein the second clock is provided by a receiving unit; and

communicating the data from the buffer to the receiving unit.

9. (previously presented) The method of claim 8, further comprising initializing at least one of a first valid write access or a first valid read access.

10. (previously presented) The method of claim 8, wherein the buffer provides an initial delay time between a first valid write access and a first valid read access.

11. (previously presented) The method of claim 10, wherein the initial delay time is dependent on a maximum expected variation between such write and read accesses.

(9) Evidence Appendix

None.

(10) Related Proceedings Appendix

None.